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| 09/918,511 | 08/01/2001 | Yuan-Tung Dai | 3313-0366P-SP | 3299 |

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| EXAMINER |
|---|
| ISAAC, STANETTA D |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2812 | |

DATE MAILED: 04/11/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/918,511 | DAI ET AL. | |
| | Examiner | Art Unit | |
| | Stanetta D. Isaac | 2812 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *06 December 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-10 and 12-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 12-37* is/are rejected.

7)☒ Claim(s) *1* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Claim Objections*

1. Claim 1 objected to because of the following informalities: a spelling error leastthe should be **least the**. Appropriate correction is required.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-10 and 12-37 are rejected under 35 U.S.C. 102(e) as being anticipated by Inoue et al. Patent Number 6,127,199.

4. Inoue discloses the method for manufacturing substantially as claimed. See **FIGS. 1-42** where Inoue teaches a method for manufacturing a thin film transistor panel, comprising at least the following steps:

providing a silicon substrate **100, 3000**;

forming a transparent insulator **120, 3100** on a front surface of said silicon substrate;

forming a plurality of thin film transistor structures **140** and a plurality of corresponding transparent electrodes **1700** on said transparent insulator;

forming a black matrix **1750** on said plurality of thin film transistor structures;

bonding a transparent substrate **180, 1900** onto the front surface of said silicon substrate;

removing said silicon substrate; and

etching said transparent insulator to expose said plurality of corresponding transparent electrodes.

5. Pertaining to claim 2, Inoue teaches a method for manufacturing a thin film transistor panel of claim 1, wherein said transparent insulator is SiOx.

6. Pertaining to claim 3, Inoue teaches a method for manufacturing a thin film transistor panel of claim 1, wherein said transparent insulator is SiN.

7. Pertaining to claim 4, Inoue teaches a method for manufacturing a thin film transistor panel of claim 1, wherein the thickness of said transparent insulator is less than 1 micrometer.

8. Pertaining to claim 5, Inoue teaches a method for manufacturing a thin film transistor panel of claim 1, wherein said transparent electrode is made of indium tin oxide.

9. Pertaining to claim 6, Inoue teaches a method for manufacturing a thin film transistor panel of claim 1, wherein said transparent substrate is a glass substrate.

10. Pertaining to claim 7, Inoue teaches a method for manufacturing a thin film transistor panel of claim 1, wherein said transparent substrate is a polymer substrate.

11. Pertaining to claim 8, Inoue teaches a method for manufacturing a thin film transistor panel of claim 1, wherein the step of removing said silicon substrate includes chemical mechanical polishing.

12. Pertaining to claim 9, Inoue teaches a method for manufacturing a thin film transistor panel of claim 1, wherein the step of removing said silicon substrate includes an etching process.

13. Pertaining to claim 10, Inoue teaches a method for manufacturing a thin film transistor panel of claim 1, further comprising forming an alignment mark on said transparent insulator.

14. Pertaining to claim 12, Inoue teaches a method for manufacturing a thin film transistor panel of claim 1, wherein the step of forming said plurality of thin film transistor structures and said plurality of corresponding transparent electrodes further comprises:

forming a transistor film and a transparent electrode on said transparent insulator;

forming a gate insulator **148, 1200a, 1200b** covering said transistor thin film and said transparent electrode;

forming a gate electrode **150, 1300a, 1300b** on said gate insulator corresponding to a position of said transistor thin film;

forming an interlayer **154, 1500** on said gate electrode and said gate insulator;

forming a metal contact layer **152, 1400a-d** on said gate insulator; and

forming a passivation layer **1600** on said metal contact layer.

15. Pertaining to claim 13, Inoue teaches a method for manufacturing a thin film transistor panel of claim 12, wherein the transistor thin film is selected from the group consisting of polycrystal silicon (pSi), polycrystal germanium (p-Ge), polycrystal silicon germanium (p-SiGe), crystal silicon (c-Si), crystal germanium (c-Ge), and crystal silicon germanium (c-SiGe).

16. Pertaining to claim 14, Inoue teaches a method for manufacturing a thin film transistor panel of claim 12, further comprising forming a color filter on said passivation layer.

17. Pertaining to claim 15, Inoue teaches a method for manufacturing a thin film transistor panel, comprising at least the following steps:

providing a silicon substrate; forming a transparent insulator on a front surface of said silicon substrate;

forming a plurality of thin film transistor structures on said transparent insulator;

bonding a transparent substrate onto the front surface of said silicon substrate;

removing said silicon substrate; and

forming a plurality of transparent electrodes corresponding to said plurality of thin film transistor structures on a bottom surface of said transparent insulator.

18. Pertaining to claim 16, Inoue teaches a method for forming a thin film transistor panel of claim 15, wherein said transparent insulator is SiO.

19. Pertaining to claim 17, Inoue teaches a method for manufacturing a thin film transistor panel of claim 15, wherein said transparent insulator is SiN.

20. Pertaining to claim 18, Inoue teaches a method for manufacturing a thin film transistor panel of claim 15, wherein the thickness of said transparent insulator is less than 1 micrometer.

21. Pertaining to claim 19, Inoue teaches a method for manufacturing a thin film transistor panel of claim 15, wherein said transparent electrode is made of indium tin oxide.

22. Pertaining to claim 20, Inoue teaches a method for manufacturing a thin film transistor panel of claim 15, wherein said transparent substrate is a glass substrate.

23. Pertaining to claim 21, Inoue teaches a method for manufacturing a thin film transistor panel of claim 15, wherein said transparent substrate is a polymer substrate.

24. Pertaining to claim 22, Inoue teaches a method for manufacturing a thin film transistor panel of claim 15, wherein the step of removing said silicon substrate includes chemical mechanical polishing.

25. Pertaining to claim 23, Inoue teaches a method for manufacturing a thin film transistor panel of claim 15, wherein the step of removing said silicon substrate includes an etching process.

26. Pertaining to claim 24, Inoue teaches a method for manufacturing a thin film transistor panel of claim 15, further comprising forming an alignment mark on said transparent insulator.

27. Pertaining to claim 25, Inoue teaches a method for manufacturing a thin film transistor panel of claim 15, further comprising forming a black matrix on said plurality of thin film transistor structures before bonding said transparent substrate onto the front surface of said silicon substrate.

28. Pertaining to claim 26, Inoue teaches a method for manufacturing a thin film transistor panel of claim 15, wherein the step of forming said plurality of thin film transistor structures and said plurality of corresponding transparent electrodes further comprises:

forming a transistor thin film on said front surface of said transparent insulator;

forming a gate insulator covering said transistor thin film and said plurality of transparent electrodes;

forming a gate electrode on said gate insulator corresponding to a position of said transistor thin film; forming an interlayer on said gate electrode and said gate insulator;

forming a metal contact layer on said gate insulator; and

forming a passivation layer on said metal contact layer.

29. Pertaining to claim 27, Inoue teaches a method for manufacturing a thin film transistor panel of claim 26, wherein said transistor thin film is selected from the group consisting of polycrystal silicon (p-Si), polycrystal germanium (p-Ge), polycrystal silicon germanium (p-SiGe), crystal silicon (c-Si), crystal germanium (c-Ge), and crystal silicon germanium (c-SiGe).

30. Pertaining to claim 28, Inoue teaches a method for manufacturing a thin film transistor panel of claim 15, further comprising forming a color filter on the bottom surface of said transparent insulator before forming said transparent electrode.

31. Pertaining to claim 29, Inoue teaches a method for manufacturing thin film transistor panel, comprising at least the following steps:

providing a silicon substrate;

bonding a transparent substrate onto a back surface of said silicon substrate;

reducing the thickness of said silicon substrate to form a layer of crystal silicon thin film;

forming a plurality of thin film transistor structures on said crystal silicon thin film; etching said thin film transistor structures and said crystal silicon thin film to form a suitable pixel via;

forming a planarization layer on said thin film transistor structures and said pixel via; and forming a plurality of transparent electrodes corresponding to the thin film transistor structures on said planarization layer.

32. Pertaining to claim 30. Inoue teaches a method for manufacturing a thin film transistor panel of claim 29, wherein the thickness of said transparent insulator is less than 1 micrometer.

33. Pertaining to claim 31, Inoue teaches a method for manufacturing a thin film transistor panel of claim 29, wherein said transparent electrode is made of indium tin oxide.

34. Pertaining to claim 32, Inoue teaches a method for manufacturing a thin film transistor panel of claim 29, wherein said transparent substrate is a glass substrate.

35. Pertaining to claim 33, Inoue teaches a method for manufacturing a thin film transistor panel of claim 29, wherein said transparent substrate is a polymer substrate.

36. Pertaining to claim 34, Inoue teaches a method for manufacturing a thin film transistor panel of claim 29, wherein the step of removing said silicon substrate includes chemical mechanical polishing.

37. Pertaining to claim 35, Inoue teaches a method for manufacturing a thin film transistor panel of claim 29, wherein the step of removing said silicon substrate includes an etching process.

38. Pertaining to claim 36, Inoue teaches a method for manufacturing a thin film transistor panel of claim 29, wherein the step of forming said thin film transistor structures further comprises:

forming a source region and a drain region on said crystal silicon thin film;

forming a gate insulator covering said transistor thin film and said transparent electrode;

forming a gate electrode on said gate insulator;

forming an interlayer on said gate electrode and said gate insulator; and

forming a metal contact layer on said gate insulator.

39. Pertaining to claim 37, Inoue teaches a method for manufacturing a thin film transistor panel of claim 29, wherein the planarization layer is also a color filter.

40. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

41. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

***Conclusion***

42. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 703-308-5871. The examiner can normally be reached on Monday-Friday 7:30am -5:30pm.

43. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Nebling can be reached on 703-308-3325. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-3432 for After Final communications.

44. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Stanetta Isaac
Patent Examiner
April 2, 2003

John F. Niebling
Supervisory Patent Examiner
Technology Center 2800